Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig.1. This sheet, which includes Fig.1, replaces the original sheet including Fig.1. In Fig.1, previously omitted elements, dielectric layer 13 and implantation well 15, have been added.

Attachment:	Replacement Sheet	1 page
	Annotated Sheet Showing Changes	1 page

REMARKS/ARGUMENTS

1. Objection to drawings under 37 CFR 1.83(a) due to incompleteness.

Examiner has objected to the drawings under 37 CFR 1.83(a) due to incompleteness. Examiner cited a limitation in claims 4 and 13 regarding an ion implantation well, and states that said well is not shown in the drawings. In addition, the dielectric layer of claims 6 and 15 must be shown in the drawings. No new matter should be entered.

Response:

Regarding objection to drawings under 37 CFR 1.83(a), replacement sheet including the ion implantation well 15 and the dielectric layer 13 is provided to replace the previous sheet of drawing. In addition, the specification has been amended in paragraph [0017] to indicate reference numerals respectively. No new matter is introduced by these amendments.

2. Objection to claims 3 and 12:

Claims 3 and 12 are objected to because of the following informalities: Each of said claims recites "inter layer" (three occurrences) which should be either "interlayer" or "inter-layer". Appropriate correction is required.

Response:

Applicants have amended claims 3 and 12 to correct the term, "inter layer" to "inter-layer". The corresponding specification, paragraph [0018], [0019] and [0020] are revised. Applicants appreciate the correction of Examiner.

3. Rejection of claims 7 and 11-13:

Claims 7 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. U.S. Patent 5,607,866 (the '866 reference). Reasons of rejection are cited on page 5-6 of above-mentioned Office Action.

Response:

Examiner notes that Sato et al. teaches a semiconductor integrated circuit device comprising a metal insulator semiconductor filed effect transistor and a resistor. The resistor includes a substrate, a p-type semiconductor region, and a pair of p^+-type semiconductor regions. Examiner states: that Sato's substrate (1A/1B) correspond to applicant's substrate of claim 7; that Sato's p-type semiconductor region (14R) correspond to applicant's high resistance region of claim 7; and that Sato's p^+-type semiconductor regions correspond to applicant's low resistance region of claim 7.

Claim 7 has been amended with incorporation of the limitation of claim 10 together with claim 8 and 9 to overcome this rejection. All amendments are fully supported by the specification and the figures. No new matter is added. The amended claim 7 is repeated below for reference:

7. (Currently amended) A resistor structure comprising:

a substrate; [[and]]

a semiconductor layer positioned on the substrate, the semiconductor layer comprising at least a high resistance region and a low resistance region;

a salicide block positioned on the portions of the semiconductor layer within the high resistance region; and

a salicide layer positioned on the portions of the semiconductor layer within the low resistance region;

wherein the semiconductor layer comprises a predetermined region overlapping the low resistance region, the junction between the low resistance region and the high resistance region, and the portions of the high resistance region adjacent to the junction between the

low resistance region and the high resistance region, and the semiconductor layer has a higher doping concentration within the predetermined region than in the other ~~regions~~ region of the semiconductor layer, and the predetermined region also overlapping the salicide layer, the junction between the salicide layer and the salicide block, and the portions of the salicide block adjacent to the junction between the salicide layer and the salicide block.

Based on the amended claim 7, the "predetermined region" should be interpreted as the heavily doped region 12b, and the other region of the semiconductor layer should be interpreted as the semiconductor region 12a. As illustrated in Fig.4, the boundary between the salicide layer and the salicide block is different from that between the high resistance region and the low resistance region. Therefore, a portion of the heavily doped region 12b is located in the high resistance region, and has a higher doping concentration than the other region of the semiconductor layer (12a). Besides, Sato et al. do not teach the resistor having a salicide block, a salicide layer, and a predetermined region overlapping the salicide layer, the junction between the salicide layer and the salicide block, and the portions of the salicide block adjacent to the junction between the salicide layer and the salicide block. Accordingly, claim 7 has been amended to patentably distinguish claim 7 from cited prior art reference.

Thus, claim 7 should be allowed over Sato. Claims 11-13 are dependent on claim 7, and should be allowed if claim 7 is found allowable. Reconsideration of claims 7, 11-13 is respectfully requested.

4. Rejection of claim 7, 11, and 13-15:

Claim 7, 11, and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa et al. U.S. Patent Application Publication 20050074929 (the '929 reference). Reasons of rejection are cited on page 6-7 of above-mentioned Office Action.

Response:

Examiner notes that Hasegawa et al. teaches a CMOS semiconductor device having a resistor circuit. Examiner states: that Hasegawa's substrate (116) correspond to applicant's substrate of claim 7; that Hasegawa's high resistance region (110) correspond to applicant's high resistance region of claim 7; and that Sato's high concentration impurity regions (108) correspond to applicant's low resistance region of claim 7.

However, claim 7 has been amended with incorporation of the limitation of claim 10 together with claim 8 and 9 to overcome this rejection. All amendments are fully supported by the specification and the figures. No new matter is added.

Moreover, Hasegawa et al. do not teach the resistor having a salicide block, a salicide layer, and a predetermined region overlapping the salicide layer, the junction between the salicide layer and the salicide block, and the portions of the salicide block adjacent to the junction between the salicide layer and the salicide block. Accordingly, claim 7 has been amended to patentably distinguish claim 7 from cited prior art reference.

Thus, claim 7 should be allowed over Hasegawa et al. Claims 11, and 13-15 are dependent on claim 7, and should be allowed if claim 7 is found allowable. Reconsideration of claims 7, 11, and 13-15 is respectfully requested.

5. Rejection to claims 8-9:

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. U.S. Patent 5,607,866 (the '866 reference) in view of Kamino et al. U.S. Patent Application Publication 20020140097 (the '097 reference).

Response:

Claims 8-9 have been cancelled, and are no longer in need of consideration.

6. Objection to claim 10:

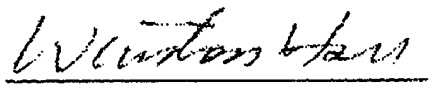
Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowed if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response:

Applicants have incorporated claim 10 into the original claim 7. As claim 10 is dependent upon claim 8 and 9, the amended claim 7 includes all limitations of the original claim 8-10. No new matter is added.

In light of above remarks and amendments to the claims, the applicants submit that all of the claims are patentably distinct from the cited prior art reference. Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Annotated Sheet Showing Changes

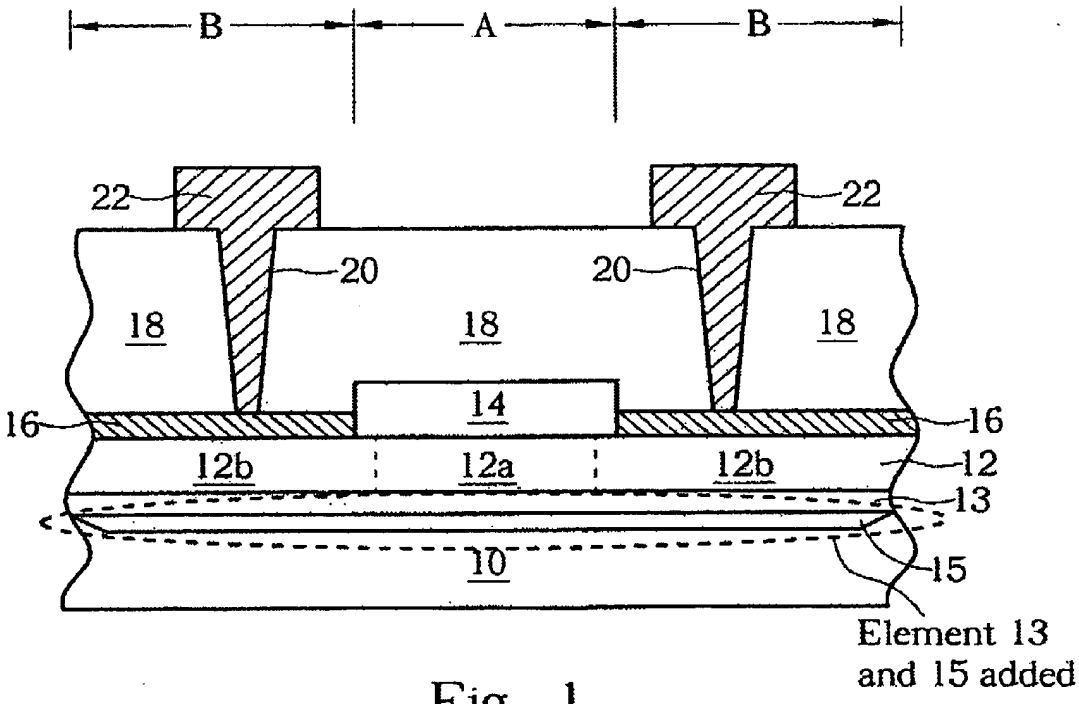

Fig. 1